REMARKS

Applicant respectfully requests reconsideration and allowance of the subject application. Claims 19 and 22 have been amended. Claims 7-13 and 19-33 are pending.

35 U.S.C. §102

Claims 19-24 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,344,663 to Slater et al. (hereinafter, "Slater"). Applicant respectfully traverses the rejection.

Claim 19 has been amended and, as amended, recites a method [portions of the amended language appear in bold italics below] comprising:

- manufacturing a fluid ejection device ***by***:
  - depositing a current prevention layer proximate a first surface of a semiconductor substrate;
  - forming first and second field effect transistors (FETs), wherein each said FET includes a gate electrode with associated active areas formed in the first surface of the semiconductor substrate having the deposited current prevention layer, wherein the current prevention layer includes a region that minimizes current flow between the active areas of the first FET with respect to the active areas of the second FET; and
  - forming a firing chamber above the current prevention layer.

Support for this amendment can be found throughout the specification. Neither Slater, nor any of the other submitted references, alone or in combination, disclose or suggest the method of manufacturing a fluid ejection device, which includes forming a firing chamber. Accordingly, for at least this reason, this claim is allowable.

Claims 20-21 and **33** depend directly from claim 19 and are allowable as depending from an allowable base claim. These claims are also allowable for their

own recited features which, in combination with those recited in claim 19, are neither shown or suggested in the references of record, either singly or in combination with one another.

Claim 22 has been amended and, as amended, recites a method [portions of the amended language appear in bold italics below] comprising:

- depositing a layer of oxide proximate a first surface of a semiconductor substrate;
- exposing a portion of the first surface of the semiconductor substrate; and
- forming a field effect transistor (FET) on the exposed portion of the first surface of the substrate having the deposited oxide layer, wherein the FET includes a gate electrode with associated active areas formed ***after the exposing*** in the first surface of the semiconductor substrate.

Support for this amendment can be found throughout the specification. Neither Slater, nor any of the other submitted references, alone or in combination, disclose or suggest these aspects.

Slater is directed to silicon carbide CMOS devices. In FIG. 3 and the discussion relating thereto, Slater describes the fabrication sequence for the CMOS device. At blocks 102-118 of FIG. 3 of Slater, active regions are formed for the silicon carbide CMOS device. Then, at block 124 of FIG. 3 of Slater, an isolation layer is deposited and etched to expose source and drain regions. Thus, Slater describes the formation of the active regions before the depositing of the isolation layer. Nowhere in Slater is there discussion, teaching or suggestion for the depositing, exposing and forming as claimed in claim 22. Accordingly, for at least this reason, claim 22 is allowable over Slater.

Claim 23 depends directly from claim 22 and is allowable as depending from an allowable base claim. This claim is also allowable for its own recited features which, in combination with those recited in claim 22, are neither shown nor suggested in the references of record, either singly or in combination with one another.

Claim 24 recites a method of making a semiconductor device comprising:

- depositing a layer of oxide proximate a first surface of a semiconductor substrate;
- exposing a portion of the first surface of the semiconductor substrate;
- forming a gate oxide layer on the exposed portion of the first surface, adjacent to the deposited oxide layer;
- forming a pair of active areas in the exposed portion of the first surface, adjacent the deposited oxide layer and gate oxide layer;
- forming a gate electrode by depositing a conductive layer over the gate oxide layer;
- depositing a dielectric layer over the gate electrode, active areas, and deposited oxide layer; and
- forming electrical contacts to the pair of active areas and the gate electrode.

Stater does not disclose these aspects.

Nowhere in Slater is there discussion, teaching or suggestion for depositing, exposing, and forming as claimed in claim 24. The Office asserted FIG. 8 as describing "depositing a layer of oxide 58", "exposing a portion of the first surface of the semiconductor substrate, i.e. exposing the portions where transistors ... to be formed", and "forming a pair of active areas 36 and 38 in the exposed portion of the first surface, adjacent the deposited oxide layer 58 and gate oxide layer 49 (FIG. 8)". However, as previously discussed, Slater describes that "[a]fter the formation of the n^+ and p^+ regions, the two devices are fabricated in the same manner". *Slater, Col. 10, Lines 18-22.* Slater then describes the following:

> After completion of the formation of the gate dielectric layer 49, the gate metal 50 and 52, is deposited and patterned. This operation is shown in block 122 of FIG. 3. After deposition of the gate material, an isolation layer 58 is deposited on the wafer and vias are etched through the isolation layer to expose portions of the n^+ and p^+ source and drain regions or the well region or the epitaxial layer. The formation of the isolation layer 58 is illustrated in FIG. 8. The isolation layer 58 is preferably formed of silicon dioxide but may be formed of any suitable insulating material such as silicon nitride. The isolation layer serves to isolate the devices from an interconnect metallization layer which is formed on the isolation layer. The formation of the isolation layer is reflected in block 124 of FIG. 3 *Slater, Col. 10, Line 62 to Col. 11, Line*

Thus, Slater describes the formation of the n^+ and p^+ source and drain regions and then the formation of the isolation layer. Claim 24 recites depositing a layer of oxide proximate a first surface of a semiconductor substrate, exposing a portion of the first surface of the semiconductor substrate, and forming a pair of active areas *in the exposed portion of the first surface*, adjacent the deposited oxide layer and gate oxide layer. Thus, in claim 24 the active areas are formed in an exposed surface of a semiconductor substrate having a deposited oxide layer. In Slater, however, n^+ and p^+ source and drain regions are formed, and then the isolation layer is formed. Accordingly, for at least this reason, claim 24 is allowable over Slater.

Claims 25-31 depend directly from claim 24 and are allowable as depending from an allowable base claim. These claims are also allowable for their own recited features which, in combination with those recited in claim 24, are

neither shown nor suggested in the references of record, either singly or in combination with one another.

35 U.S.C. §102

Claims 24-33 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,485,132 to Hiroki et al. (hereinafter, "Hiroki"). Applicant respectfully traverses the rejection.

Claim 24, as previously stated, recites depositing a layer of oxide proximate a first surface of a semiconductor substrate, exposing a portion of the first surface of the semiconductor substrate, and forming a pair of active areas *in the exposed portion of the first surface*, adjacent the deposited oxide layer and gate oxide layer. Hiroki does not disclose these aspects.

Hiroki is directed to a liquid discharge head, recording apparatus and method for manufacturing liquid discharge heads. The Office asserted FIG. 4 and the related text as describing "depositing a layer of oxide 416 proximate a first surface of a semiconductor substrate", "exposing a portion of the first surface of the semiconductor substrate, exposing the portions where transistors 450 and 451 to be formed", and "forming a pair of active areas 405 and 406 in the exposed portion of the first surface, adjacent the deposited oxide layer 416 and gate oxide layer 408, wherein the active areas 405 and 406 are formed by impurity implant and diffusion (col. 9, lines 203)". *Office Action dated October 31, 2003, Page 5.* The interlayer insulation layer 416 of Hiroki, however, is installed "[a]fter each of the elements is formed" as shown in the following excerption. *Hiroki, Col. 9, Line 20.*

> Using the general MOS (Metal Oxide Silicon) process the impurity installation such as ion plantation and its diffusion

are conducted to form the p-MOS on the n type well region 402 of the silicon substrate 401, which is p conductor, and the n-MOS 451 on the p type well region 403, respectively. The p-MOS 450 and the n-MOS 451 comprise the gate wiring 415, the source region 405 where the n-type or p-type impurity is implanted, the drain region 406, and some others, which are formed by polysilicon deposited by means of the CVD method in a thickness of 4,000 .ANG. or more and 5,000 .ANG. or less through the gate insulation film 408 of several hundreds A, respectively. Then, the C-MOS logic is structured by these p-MOS and n-MOS.

Also, on the p-well substrate, the n-MOS transistor is arranged for use of element driving, which comprises the drain region 411, the source region 412, the gate wiring 413, and others formed also by the process of impurity installation and diffusion or the like.

Between the respective elements, the oxidized film separation region 453 is formed by means of the field oxidation in a thickness of 5,000 .ANG. to 10,000 .ANG. to separate each of the elements, respectively. The field oxidation film functions as the first heat accumulation layer 414 for the thermal activation portion 108.

After each of the elements is formed, there is installed the interlayer insulation film 416 formed by PSG (Phospho-Silicate Glass) film, BPSG (Boron-doped Phospho-Silicate Glass) film, or the like, prepared by the CVD method in a thickness of approximately 7,000 .ANG.. Further, subsequent to the smoothing process or the like that has been executed by heat treatment on the interlayer insulation film 416, wiring is made through the contact hole on the first wiring layer 417 formed by the Al electrodes. Then, the interlayer insulation film 418, which is formed by SiOz film or the like prepared in a thickness of 10,000 .ANG. to 15,000 .ANG., is installed by plasma CVD. Then, furthermore, the resistive layer 104, which is formed by TaN.sub.0.8,hex film prepared in a thickness of approximately 1,000 .ANG., is installed by DC sputtering method. This resistive layer 104 is partly in contact with the first wiring layer 417 by way of the through hole. After that, although not shown, the second wiring layer is formed with Al electrodes to serve as wiring to each of the heat generating members. *Hiroki, Col. 8, Line 63 to Col. 9, Line 38.*

Thus, Hiroki, describes "impurity installation such as ion implantation and its diffusion are conducted to form the p-MOS on the n type well region 402 of the silicon substrate 401, which is p conductor, and the n-MOS 451 on the p type well region 403, respectively", and then "[a]fter each of the elements is formed, there is installed the interlayer insulation film 416". *Hiroki, Col. 8, Lines 63-67 and Col. 9, Lines 20-21.* Claim 24 recites depositing a layer of oxide proximate a first surface of a semiconductor substrate, exposing a portion of the first surface of the semiconductor substrate, and forming a pair of active areas *in the exposed portion of the first surface*, adjacent the deposited oxide layer and gate oxide layer. Thus, in claim 24 the active areas are formed in an exposed surface of a semiconductor substrate having a deposited oxide layer. In Hiroki, however, the interlayer insulation film is installed after each of the elements is formed. Accordingly, for at least this reason, claim 24 is allowable over Hiroki.

Claims 25-31 depend directly from claim 24 and are allowable as depending from an allowable base claim. These claims are also allowable for their own recited features which, in combination with those recited in claim 24, are neither shown nor suggested in the references of record, either singly or in combination with one another.

35 U.S.C. §102

Claims 7, 9-13 and 32 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,200,862 to Gardner et al. (hereinafter, "Gardiner"). Applicant respectfully traverses the rejection.

Claim 7 recites a method of making a semiconductor device comprising:

- depositing a layer of oxide proximate a first surface of a semiconductor substrate;
- forming a gate oxide layer on the first surface, adjacent to the deposited oxide layer;
- forming a pair of active areas in the first surface, adjacent the deposited oxide layer and gate oxide layer;
- forming a gate electrode by depositing a conductive layer over the gate oxide layer;
- depositing a dielectric layer over the gate electrode, active areas, and deposited oxide layer; and
- forming electrical contacts to the pair of active areas and the gate electrode.

Gardner does not disclose these aspects.

Gardiner is directed to a mask for asymmetrical transistor formation with paired transistors. Gardiner discloses the first step for producing the transistor as follows:

> Substrate 10 has already had formed therein, e.g., by ion implantation, a channel region 14, a punch-through region, and a well region. (Only the channel region 14 is illustrated.) The substrate can be doped with arsenic or phosphorous ions to form an n-doped channel regions (or n-channel regions). The substrate can be doped with boron ions to form a p-doped channel (or p-channel) regions. *Gardiner, Col. 3, Lines 24-31.*

Gardiner then discloses that "[a]fter formation of doped regions in the substrate 10, a gate dielectric layer 22, of 10-30 ANG. is formed by oxide growth, plasma deposition, or low pressure chemical vapor deposition." *Gardiner, Col 3, Lines 52-55.* After which, Gardiner discloses a patterning of layer 30 for ion bombardment to form a resulting device having asymmetric source/drain regions. *See Gardiner, Col. 4, Lines 14-36.* Finally, Gardiner discloses formation of a dielectric layer as follows:

> The photoresist regions 30 are removed and a dielectric layer 40, typically silicon oxide is formed and planarized. Vias are formed in the dielectric layer 40 exposing the surfaces of the substrate source/drain regions 28[1], 34 and the surfaces of the

gate electrode of gate structure 20. *Gardiner, Col 4, Lines 40-44.*

Thus, Gardiner discloses the formation of the dielectric layer 40 after the formation of the source/drain regions.

Nowhere in Gardiner is there discussion, teaching or suggestion for depositing a layer of oxide proximate a first surface of a semiconductor substrate and forming a pair of active areas in the first surface, ***adjacent the deposited oxide layer*** and gate oxide layer as recited in claim 7. For these reasons, claim 7 is allowable over Gardiner. Applicant respectfully requests that the §102 rejection of claim 7 be withdrawn.

Claims 8-13 depend from claim 7 and are allowable by virtue of this dependency.

35 U.S.C. §103

Claim 8 is rejected under 35 U.S.C. §103 as being unpatentable over Gardner in view U.S. Patent Application Publication No.: US2003/0081070 A1 to Liu et al. (hereinafter Liu). The Applicant respectfully traverses the rejection.

Claim 8 depends from claim 7. As previously stated in relation to claim 7, Gardner does not disclose, teach or suggest depositing a layer of oxide proximate a first surface of a semiconductor substrate and forming a pair of active areas in the first surface, adjacent ***the deposited oxide layer*** and gate oxide layer as recited in claim 7. Liu does not correct the deficiencies of the Gardner reference. For these reasons, claim 8 is allowable over Gardiner in view of Liu. Applicant respectfully requests that the §103 rejection of claim 8 be withdrawn.

Conclusion

All pending claims 7-13 and 19-33 are in condition for allowance. Applicant respectfully requests reconsideration and prompt issuance of the subject application. If any issues remain that prevent issuance of this application, the Examiner is urged to contact the undersigned attorney before issuing a subsequent Action.

Respectfully submitted,

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By: _____

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